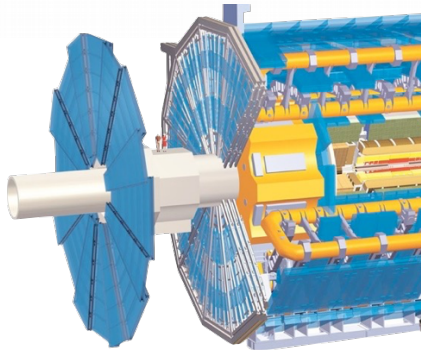
TEXAS
The University of Texas at Austin

ATLAS EXPERIMENT



Update

Ray Xu

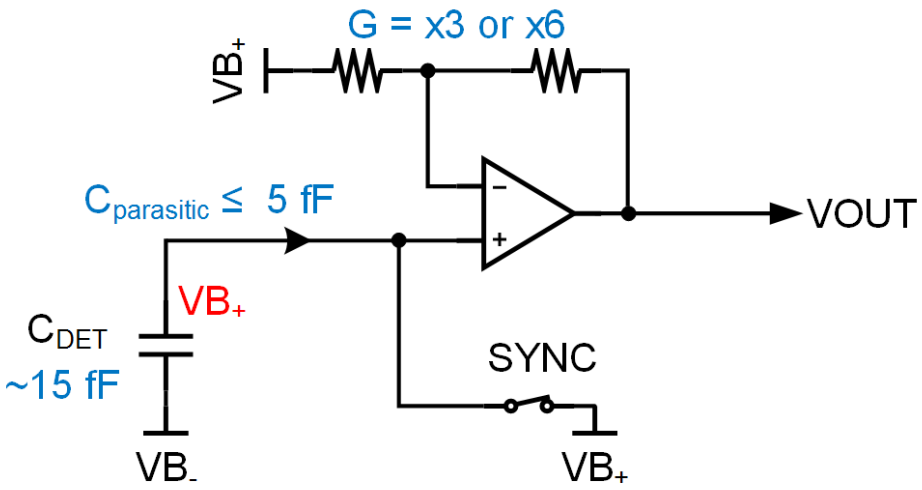
Apr 14, 2017

Outline

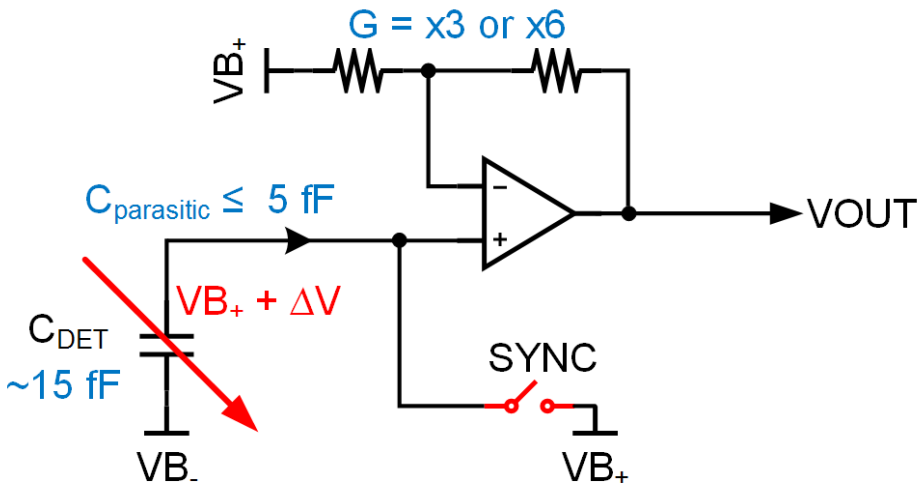
- Electrometer OTA (overdue)
  - Operation
  - Specs
- Overview of SEU readout system
- Layout update

Electrometer Operation

SYNC ("RESET") Phase



DETECT Phase



Electrometer Specs

- General
  - 3x or 6x gain (Selected by scan chain)
  - 1 fF input capacitance
  - In. Noise (1 Hz → 10 GHz): 2 mVrms
  - Out. Noise (1 Hz → 10 GHz): 700uVrms
  - In. Noise (sampled 40MSPS, 1 Hz → 20 MHz): 186uVrms
  - Out. Noise (samp. 40MSPS, 1 Hz → 20 MHz): 575uVrms
  - (Noise simulated w/ 20pF output load)
  - Low-parasitic & low-charge injection SYNC switch (ΔV ~ 20uV)

Electrometer Specs (cont.)

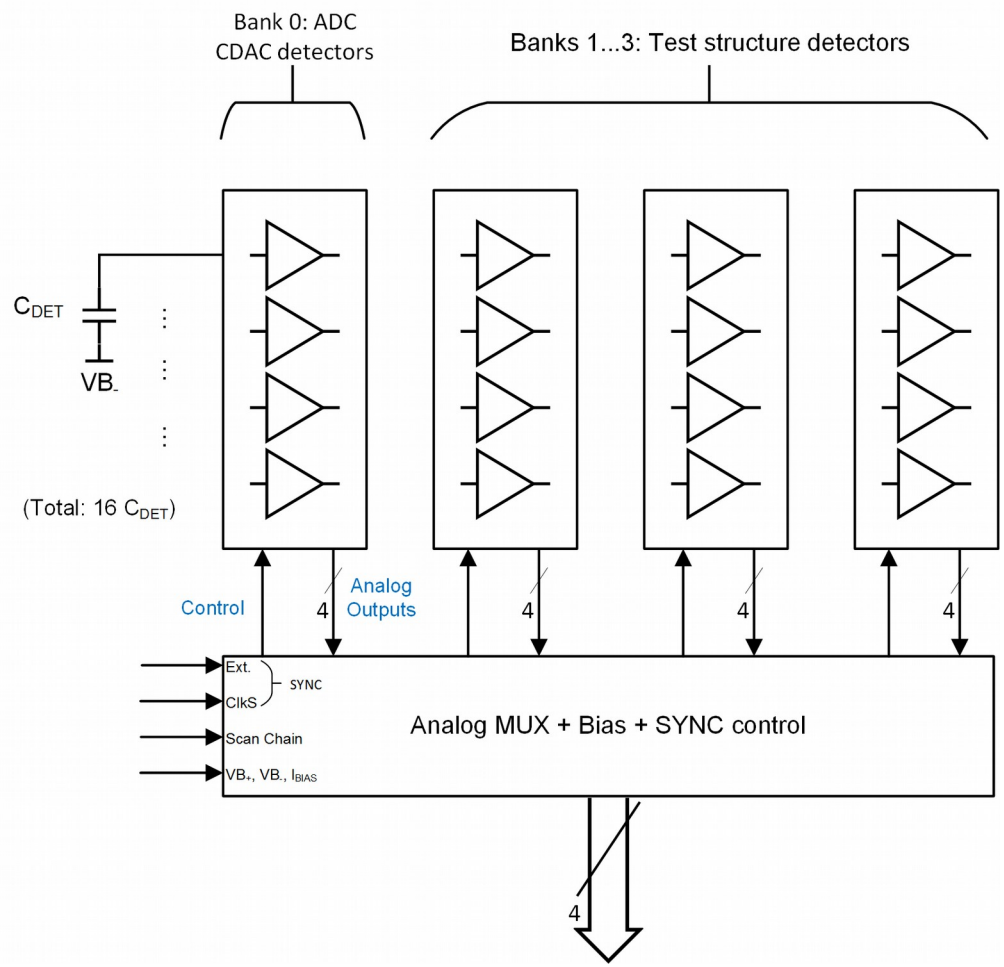
- Post-layout OTA R+C+CC extraction
- 5pF load BW
  - Slow-slow corner
    - G = x3: 240 MHz, PM 55 deg
    - G = x6: 137 MHz, PM 50 deg
  - Fast-fast
    - G = x3: 434 MHz, PM 50 deg
    - G = x6: 232 MHz, PM 50 deg
- 20pF load BW (only typ-typ corner)
  - G = x3: 187 MHz, PM 73 deg, 1.5 nS r/f time
  - G = x6: 116 MHz, PM 63 deg, 2.2 nS r/f time

Electrometer Design

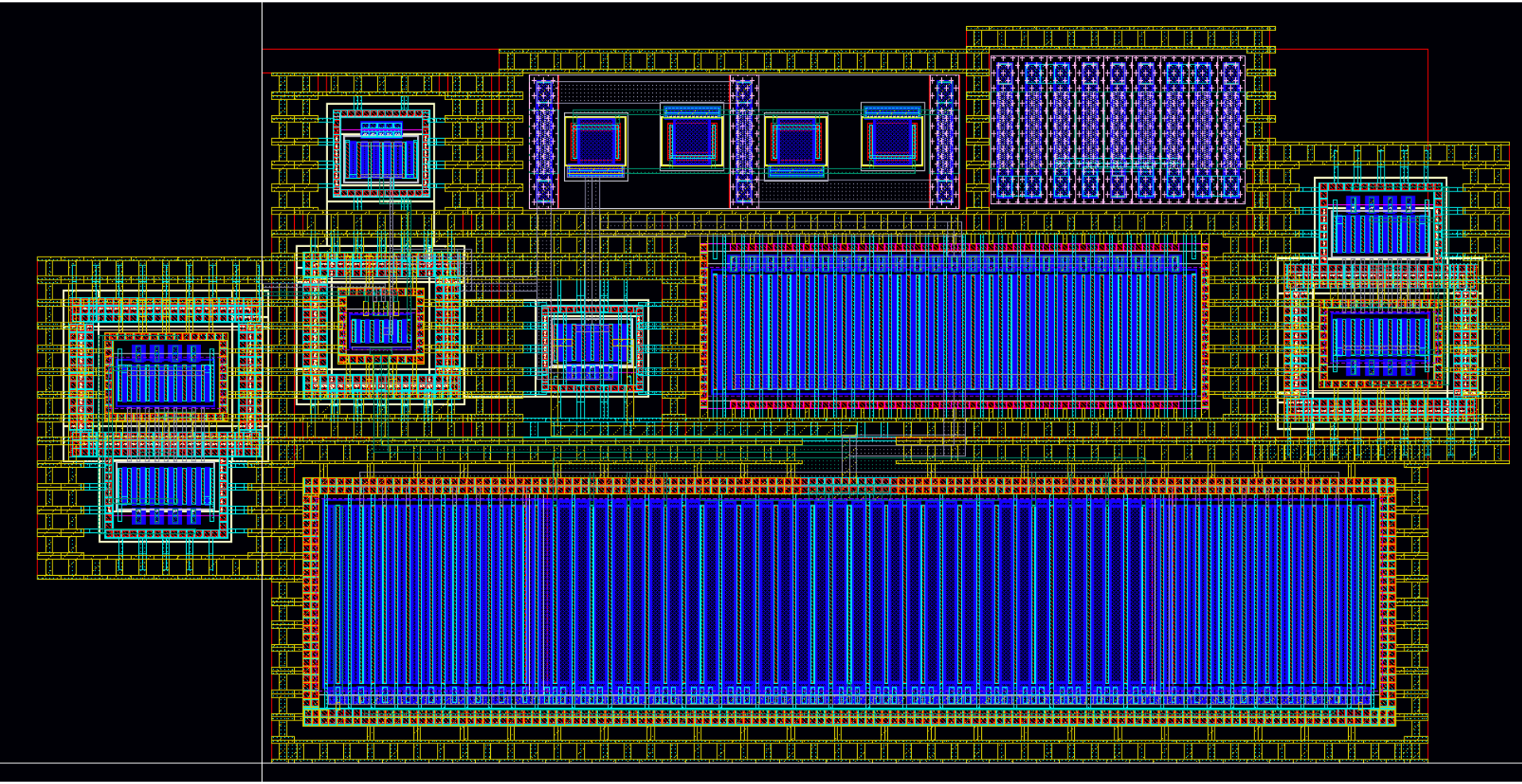
- Does not use traditional sw-cap integrator
  - Possible to discern between SEU hitting detector cap vs. amplifier circuitry…that's the theory, at least.
  - Compatibility with all capacitances for Cdet
  - No clocks, latches, or states (all cont. time)
- Caveats: (to be addressed in next tapeout?)
  - 30 dB open-loop gain → possible accuracy issues
  - Voltage offsets per input and across multiple OTA's:
  - Just have one channel/electrometer/OTA in the future?
  - Characterize test chip before irradiation…

SEU Readout

- Total power draw: ~5mW
- Additional built-in functionality for testing/characterization purposes



Electrometer Layout



20um x 40um

To-do

- Next few days
  - Piece together 4 electrometers (a “Bank”)
  - Start layout on analog MUX + bias distribution + SYNC control (about a dozen unique transistors)
  - CDAC detector cells?